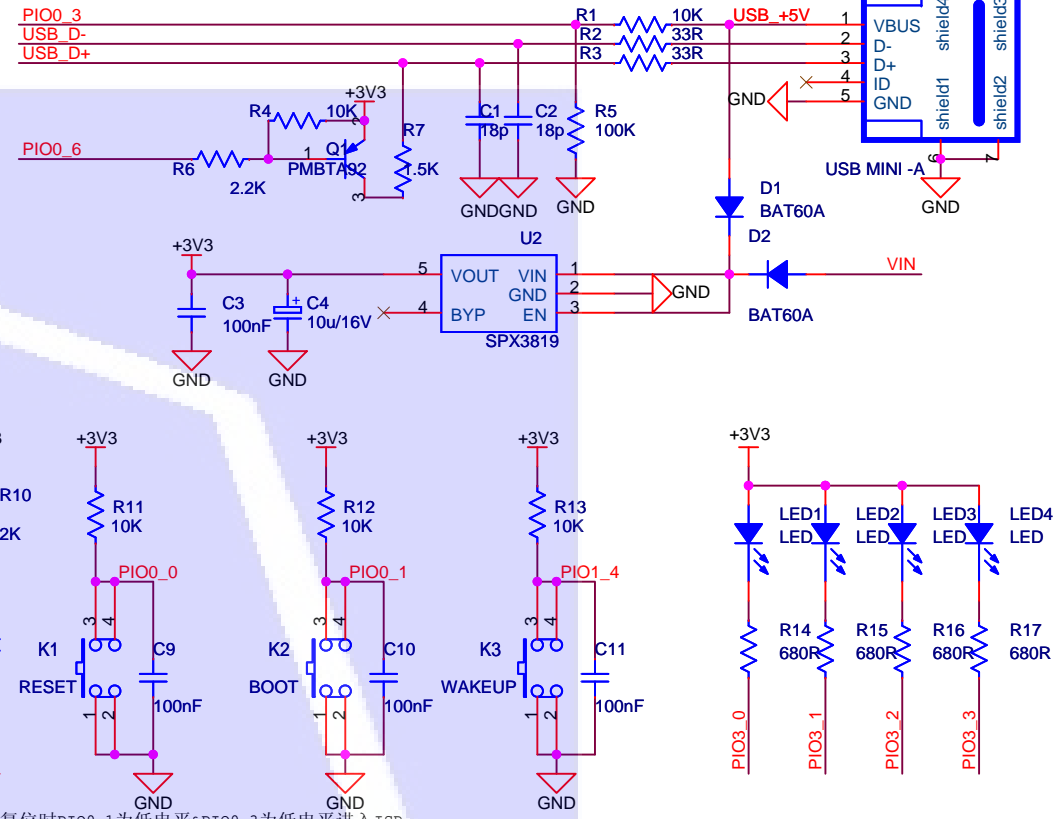
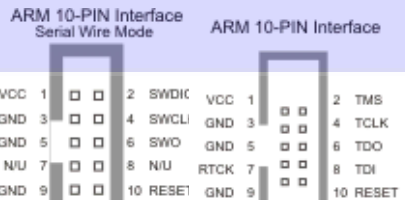
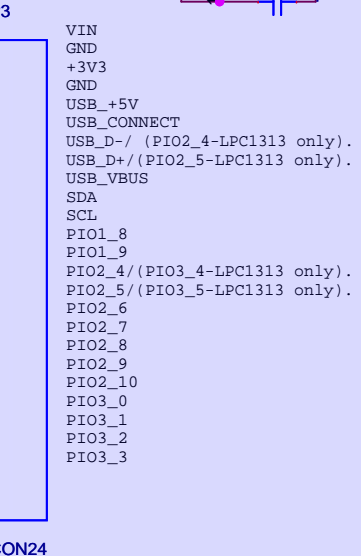
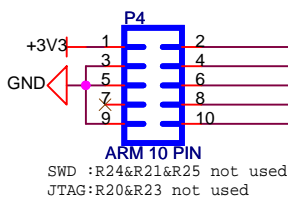
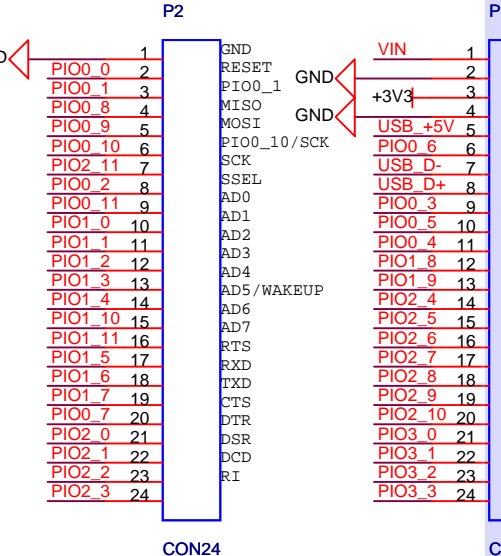
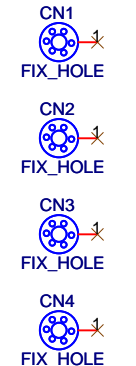
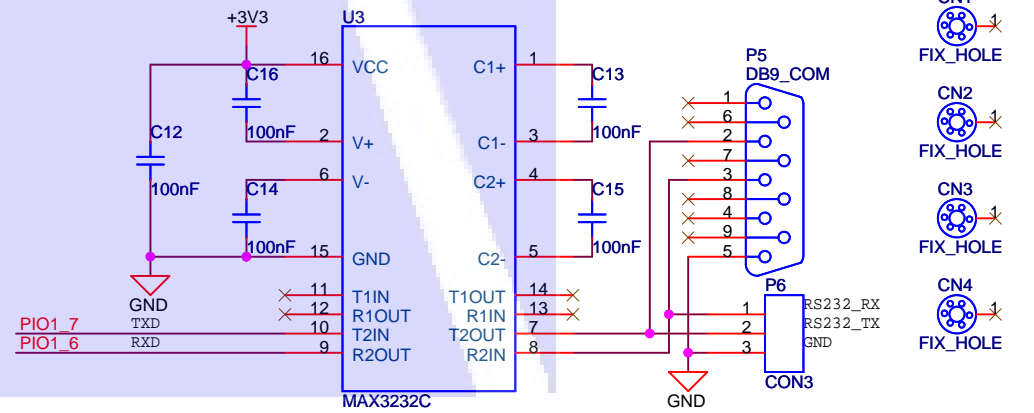


PIO0_0	3	RESET/PIO0_0	2	PIO2_0	2	PIO2_0
PIO0_1	4	PIO0_1/CLKOUT/CT32B0_MAT2	13	PIO2_1	13	PIO2_1
PIO0_2	10	PIO0_2/SSEL/CT16B0_CAPO	26	PIO2_2	26	PIO2_2
PIO0_3	14	PIO0_3	38	PIO2_3	38	PIO2_3
PIO0_4	15	PIO0_4/SCL	18	PIO2_4	18	PIO2_4
PIO0_5	16	PIO0_5/SDA	21	PIO2_5	21	PIO2_5
PIO0_6	22	PIO0_6/SCK	1	PIO2_6	1	PIO2_6
PIO0_7	23	PIO0_7/CTS	11	PIO2_7	11	PIO2_7
PIO0_8	27	PIO0_8/MISO/CT16B0_MAT0	12	PIO2_8	12	PIO2_8
PIO0_9	28	PIO0_9/MOSI/CT16B0_MAT1/TRACE_SWV	24	PIO2_9	24	PIO2_9
PIO0_10	29	TCK/PIO0_10/SCK/CT16B0_MAT2	25	PIO2_10	25	PIO2_10
PIO0_11	32	TDI/PIO0_11/AD0/CT32B0_MAT3	31	PIO2_11	31	PIO2_11
PIO1_0	33	TMS/PIO1_0/AD1/CT32B1_CAPO	36	PIO3_0	36	PIO3_0
PIO1_1	34	TDO/PIO1_1/AD2/CT32B1_MAT0	37	PIO3_1	37	PIO3_1
PIO1_2	35	TRST/PIO1_2/AD3/CT32B1_MAT1	43	PIO3_2	43	PIO3_2
PIO1_3	39	SWD/PIO1_3/AD4/CT32B1_MAT2	48	PIO3_3	48	PIO3_3
PIO1_4	40	PIO1_4/AD5/CT32B1_MAT3/WAKEUP	19	USB_D-	19	USB_D-
PIO1_5	45	PIO1_5/RTS/CT32B0_CAPO	20	USB_DP	20	USB_DP
PIO1_6	46	PIO1_6/RXD/CT32B0_MAT0	8	VDDIO	8	VDDIO
PIO1_7	47	PIO1_7/TXD/CT32B0_MAT1	44	VDDCORE	44	VDDCORE
PIO1_8	9	PIO1_8/CT16B1_CAPO	5	VSSIO	5	VSSIO
PIO1_9	17	PIO1_9/CT16B1_MAT0	41	VSS	41	VSS
PIO1_10	30	PIO1_10/AD6/CT16B1_MAT1	6	XTALIN	6	XTALIN
PIO1_11	42	PIO1_11/AD7	7	XTALOUT	7	XTALOUT

LPC1343



复位时PIO0\_1为低电平&PIO0\_3为低电平进入ISP。  
复位时PIO0\_1为低电平&PIO0\_3为高电平进入USB boot loader。  
On the WAKEUP pin(PIO1\_4), transition from HIGH to LOW,Wake up the chip from Deep power-down mode.



Title		
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